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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/522,335	01/25/2005	Yasushi Inagaki	264533US90PCT	8804

22850 7590 06/15/2007
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EXAMINER	
GETACHEW, ABIY	
ART UNIT	PAPER NUMBER
2841	

NOTIFICATION DATE	DELIVERY MODE
06/15/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/522,335	INAGAKI ET AL.	
	Examiner	Art Unit	
	Abiy Getachew	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01/25/2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

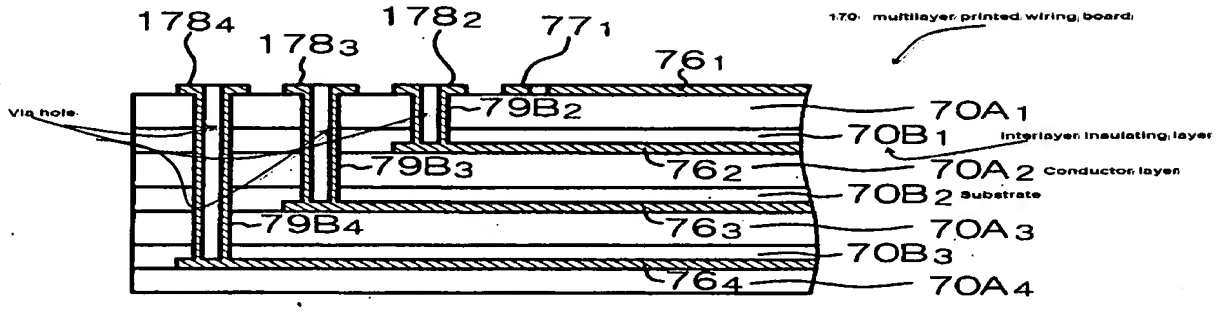
Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Azuma et.al. (US 2004/0108862 A1). DR 6/11/07

Regarding claim 1 Azuma et.al. Discloses, a multilayer printed wiring board (Figure 23 A Element 170) comprising a core substrate (Figure 23 A Element 70 B2) first conductor layer (Figure 23 A Element 70A2) having a plurality of conductor circuit formed on a core substrate(Figure 23 A Element 70 B2), and said core substrate (Figure 23 A Element 70 B2) , a second conductor layer (Figure 23 A Element 70 A2) having a plurality of conductive circuit formed on said interlayer insulating layer (Figure 23 A Element 70 B1) and a via hole structure (178) electrically connecting one of said conductor circuit of said second conductor layer (Figure 23 A Element 70 A2) being electrically connected through a via hole (Figure 23 A Element 79 B2) wherein a thickness of the conductor layer (Figure 23 A Element 70 A2) , where said first has a thickness which is larger then a thickness of the said second conductor layer on the said interlayer insulating layer (Figure 23 A Element 70 B1).



Regarding claim 2 Azuma et.al. discloses, The multilayer printed wiring board (Figure 23 A Element 170) wherein said thickness of said first conductor layer (Figure 23 A Element 70A2) on said core substrate (Figure 23 A Element 70B2) is α 1,said of said thickness of said conductor layer (Figure 23 A Element 70A1) on the interlayer insulating layer (Figure 23 A Element 70B2) is α 2, α 1 and α 2 satisfy. [Column 10 paragraph 2 section 0101]

Regarding claim 3 as applied claim above Azuma et.al. discloses, wherein said al thickness of said first conductor layer on said core substrate is α1 said thickness of said second conductor layer on said interlayer is α 2 and said α1 satisfies satisfy < α1 ≤ α 40 α 2. [Column 10 paragraph 2 section 0101]

Regarding claim 4 as applied claim above Azuma et.al. discloses wherein the first conductor layer (Figure 23 A Element 70A1) of said core substrate (Figure 23 A Element 70B2) [Column 4 paragraph 2 section 0033, i.e. power supply layer is formed in the internal layer, plate, the first and second electrodes may be formed in part of the ground layer or the power supply layer]

Regarding claim 5 as applied claim above Azuma et.al. discloses, further comprising capacitor mounted on second conductor layer (Figure 23 A Element 70 A2). [Column 3 paragraph 6 section 0030]

Regarding claim 6 as applied claim above Azuma et.al. discloses a multilayer printed wiring board (Figure 23 A Element 170) comprising, an interlayer insulating layer (Figure 23 A Element 70B1) conductor layer formed over said conductor layer (Figure 23 A Element 70 A2) wherein said core substrate (Figure 23 A Element 70B2) is a multilayer core substrate [Column 19 paragraph 3 section 0225] (Figure 23 A Element 70B2) and a through hole structure formed through said interlayer insulating layer and electrically connecting one of said conductor circuits of said at least one inner conductor layer and one of said conductor circuits of said conductor layer (Figure 23 A Element 70A2) formed over said core substrate (Figure 23 A Element 70B2), the at least inner layer of said conductor layer (Figure 23 A Element 70A2) on a surface of said core substrate (Figure 23 A Element 70B2) include a power supply layer or an earth.[Column 4 paragraph 2 section 0033]

Regarding claim 7 Azuma et.al. discloses the multilayer printed wiring board (Figure 23 A Element 170) according to claim 6, wherein said at least one inner conductor layer of said inner layer of said core substrate comprises power supply layer earth, and said core substrate and comprise a signal line.[Column 2 paragraph 3 section 0013]

Regarding claim 8 as applied claim above Azuma et.al. discloses wherein a thickness of the conductor layer (Figure 23 A Element 70A1) on said core substrate (Figure 23 A Element 70B2) is larger than a thickness of the conductor layer (Figure 23 A Element 70A1) on the interlayer-insulating layer (Figure 23 A Element 70B1). [Column 10 paragraph 2 section 0101]

Regarding claim 9 as applied claim above Azuma et.al. discloses wherein the conductor layer (Figure 23 A Element 70A1) as the inner layer of said core substrate (Figure 23 A Element 70B2) is not less then two-conductor layers (Figure 23 A Element 70A1). [Column 1 paragraph 3 section 0004]

Regarding claim 10 as applied claim above Azuma et.al. discloses wherein said core substrate (Figure 23 A Element 70B2) is constituted so that the conductor layer (Figure 23 A Element 70A1) as said inner layer is formed on each surface of an electrically isolated metallic plate through a resin layer and so that said conductor layer (Figure 23 A Element 70A1) on the surface layer is formed outside of the conductor layer (Figure 23 A Element 70A1) as the inner layer through the resin layer. [Column 1 paragraph 2 section 0002]

Regarding claim 11 as applied claim above Azuma et.al. discloses wherein said core substrate (Figure 23 A Element 70B2) comprises a thick conductor layer (Figure 23 A Element 70A1) as the inner layer and a thin conductor layer as the conductor layer on the surface layer. [Column 10 paragraph 2 section 0101]

Regarding claim 12 as applied claim above Azuma et.al. discloses, wherein the conductor layer (Figure 23 A Element 70A1) of said core substrate (Figure 23 A Element 70B2) is the conductor layer (Figure 23 A Element 70A1) for power supply layer or the conductor layer foe an earth. [Column 4 paragraph 2 section 0033]

Regarding claim 13 as applied claim above Azuma et.al. discloses, wherein a capacitor is mounted on a surface of the multilayer printed (Figure 23 A Element 170) wiring board. [Column 3 paragraph 6 section 0030]

Regarding claim 14 as applied claim above Azuma et.al. discloses, wherein a thickness of the conductor layer on said core substrate is larger than a thickness of the conductor layer on the interlayer-insulating layer. [Column 10 paragraph 2 section 0101]

Regarding claim 15 as applied claim above Azuma et.al. discloses wherein the conductor layer (Figure 23 A Element 70A1) as the inner layer of said core substrate (Figure 23 A Element 70B2) is not less than two conductor layers (Figure 23 A Element 70A1). [Column 1 paragraph 3 section 0004]

Regarding claim 16 as applied claim above Azuma et.al. discloses, wherein said core substrate (Figure 23 A Element 70B2) is constituted so that the conductor layer (Figure 23 A Element 70A1) as said inner layer is formed on each surface of an electrically isolated metallic plate through a resin layer and so that said conductor layer (Figure 23 A Element 70A1) on the surface layer is formed outside of the conductor layer (Figure 23 A Element 70A1) as the inner layer through the resin layer. [Column 1 paragraph 2 section 0002]

Regarding claim 17 as applied claim above Azuma et.al. discloses, further comprising a second conductor layer (Figure 23 A Element 70 A2) having a plurality of conductor circuit formed over said interlayer insulating layer(Figure 23 A Element 70 B1) ,wherein said conductor layer (Figure 23 A Element 70A1) formed on a surface of said core substrate(Figure 23A Element 70B2), said at least one inner layer of said core substrate, said ate least inner core substrate (Figure 23A Element 70B2) has a thickness which is larger than a thickness of the conductor layer formed on the surface of said core substrate (Figure 23A Element 70B2), and the thickness of said conductor

layer formed on the surface of said core substrate is larger than a thickness of the second conductor layer (Figure 23 A Element 70 A2). [Column 10 paragraph 2 section 0101]

3. Claims 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Azuma et al. (US 2004/0108862 A1).

Regarding claim 18 Azuma et al. Discloses A multilayer printed wiring board (Figure 23 A element 170) a core substrate (Figure 23 A Element 70 B2) and a multilayered structure formed (See Figure 23 A) on said core substrate (Figure 23 A Element 70 B2) and including a first conductor layer (Figure 23 A Element 70 A2) having a plurality of conductor circuits formed on said core substrate (Figure 23 A Element 70 B2), at least one interlayer insulating layer (Figure 23 A Element 70 B1) formed over said first conductor layer (Figure 23 A Element 70 A2), and a second conductor layer (Figure 23 A Element 70 A1) having a plurality of conductor circuits formed (See Figure 23 A) on said at least one interlayer insulating which is layer, wherein said first conductor layer on said core substrate (Figure 23 A Element 70 B2) has a thickness larger than a thickness (See Figure 23 A) of said second conductor layer on said at least one interlayer insulating layer (Figure 23 A Element 70 B1).

Regarding claim 19 as applied claim 18 above Azuma et.al. Discloses, wherein said thickness of said first conductor layer (Figure 23 A Element 70 A1) on said core substrate is α1, said thickness of said second conductor layer (Figure 23 A Element 70 A1) on said interlayer insulating layer is α 2, α 1 and α 2 satisfy $\alpha 2 < \alpha 1 \leq \alpha$ 40 α. [Column 10 paragraph 2 section 0101]

Regarding claim 20 as applied in above claim 18 Azuma et al. discloses said thickness of said first conductor layer (Figure 23 A Element 70 A1) on said core substrate (Figure 23 A Element 70 B2) is α1 said thickness of said second conductor layer insulating layer is α2 and said α1 satisfies 2 α2 < 40 α2. [Column 10 paragraph 2 section 0101]

Response to Arguments

4. Applicant's arguments filed 03/05/2007 have been fully considered but they are not persuasive.

Applicants argue that "Azuma et.al. teaches neither "a first conductor layer...; a second conductor layer ..., wherein said first conductor layer on said core substrate has a thickness which is larger than a thickness of said second conductor layer on said interlayer insulating layer" as recited in amended Claim 1, nor "a core substrate comprising a multilayer core substrate comprising not less than three layers including at least one inner conductor layer having a plurality of conductor circuits ..., wherein the at least one inner conductor layer of said core "

In response to the above argument' Applicants attention respectfully directed to (See Figure 23 A) i.e. a multilayer printed wiring board (Figure 23 A Element 170) comprising an interlayer insulating layer (Figure 23 A Element 70B1) and a conductor layer (Figure 23 A Element 70A2) formed on a core substrate (Figure 23 A Element 70 B2), the conductor layer (Figure 23 A Element 70 A2) being electrically connected through a via hole (Figure 23 A Element 79 B2) wherein a thickness of the conductor layer (Figure 23 A Element 70 A2) on said core substrate (Figure 23 A Element 70 B2)

is larger than a thickness of the conductor layer (Figure 23 A Element 70 A1) on the interlayer insulating layer (Figure 23 A Element 70 B1).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abiy Getachew whose telephone number is (571) 272 6932. The examiner can normally be reached on Monday to Friday 8Am to 4:30Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean A. Reichard can be reached on (571) 272 1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Abiy Getachew
Examiner
Art Unit 2841

A.G.
May 29, 2007

DEAN A. REICHARD
SUPERVISORY PATENT EXAMINER
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6/11/07